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(54) **Non-volatile memory device with configurable row redundancy**

(57) This invention relates to a non-volatile memory device (20) with configurable row redundancy, comprising:

- a non-volatile memory (11) comprising of at least one matrix (11') of memory cells and at least one matrix (11") of redundant memory cells, both organised into rows and columns;
- row and column decoding circuits (12,13);
- read and modify circuits for reading and modifying data stored in the memory cells; and
- at least one associative memory matrix (14), also organised into rows and columns, able to store the addresses of faulty rows, and control circuits for controlling the associative memory matrix.

The memory device (20) of this invention further comprises:

- at least one circuit for recognising and comparing selected row addresses (ADr) with faulty row addresses (ADrr) contained in the associative memory matrix (14), such as to produce de-selection of the faulty row and selection of the corresponding redundant cell row in the event of a valid recognition; and
- at least one configuration register (17), also comprising a matrix of non-volatile memory cells, and associated control circuits.

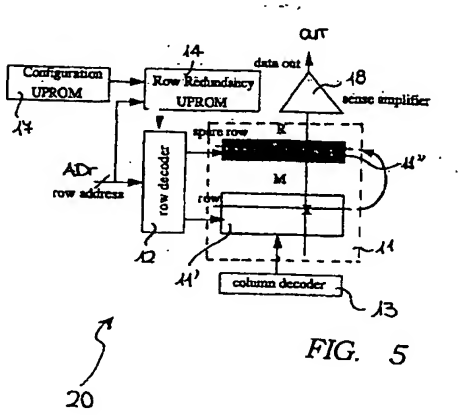

FIG. 5

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Description

Field of the Invention

[0001] This invention relates to a non-volatile memory device with configurable row redundancy.

[0002] Specifically, the invention relates to a non-volatile memory device with configurable row redundancy, comprising:

- a non-volatile memory, itself comprising at least one matrix of memory cells and at least one matrix of redundant memory cells, both organised into rows and columns;
- row and column decoding circuits;
- read and modify circuits for reading and modifying data stored in the memory cells; and
- at least one associative memory matrix, also organised into rows and columns, able to store the addresses of faulty rows and related control circuits for controlling the associative memory matrix.

[0003] The invention relates, particularly but not exclusively, to semiconductor non-volatile memory devices which are electrically programmable and fabricated with CMOS technology, and the following description is made with reference to this field of application for convenience of explanation only.

Prior Art

[0004] As it is well known, a semiconductor non-volatile memory device of the so-called "multimegabit" type, such as EEPROMs or Flash EPROMs, basically comprises a matrix of memory cells which accounts for a good proportion of the device area, specifically 40 to 70% of its total area.

[0005] The applications of such memory devices impose perfect performance of all the memory cells in the matrix during the device operation phases (reading, programming, erasing). In principle, the presence of at least one inoperative memory cell, commonly defined as "bit-fail", is sufficient to put the whole device out of use.

[0006] This requisite for utmost reliability of the memory device taxes the manufacture of this type of integrated device, because a generic memory cell in a batch has a not null probability of turning up defective. In particular, the main causes of bit-fails are connected to the technological process used to fabricate the integrated device, e.g. conductive layers shorted together, variations in the process parameters, breakdown of dielectric layers, and so on.

[0007] Lacking arrangements to detect and correct bit-fails, the percentage of devices with properly performing memory cells in a chosen fabricating batch would be low to qualify for mass production methods. This percentage shows the so called prime yield of the fabricating batch and plays a very important role in the whole manufacturing process.

[0008] In memory devices, this yield is actually dependent on the faultiness spread not only through the cell matrix interior, but also through ancillary circuits to such matrix. However, in consideration of the large area occupied by the memory, the reduced yield in devices of this type is mainly due to faults occurring within the matrix.

[0009] Suitable circuit arrangements for the detection and the correction of bit-fail are therefore employed to increase the yield in integrated memory devices.

[0010] According to a commonly used technique, spare memory cells are provided to replace those cells which have been found faulty in the matrix.

[0011] These spare memory cells, usually called redundant, are identical to the matrix memory cells they have to replace, and are suitably controlled by dedicated control circuits added to the standard device circuitry.

[0012] In particular, the memory layout prompts the use of entire redundant cell rows or columns, so that corresponding rows or columns of the memory matrix can be replaced even on the occurrence of only one bit-fail therein. In this way, a good compromise can be made between fault-correcting capability and the requested area to perform redundancy control circuits.

[0013] The choice of the type of layout of redundant cells for use in a memory device, e.g. row redundancy or column redundancy, or both, is essentially tied to the knowledge of the distribution and typology of the faults appearing in the matrix for a given technological integration process.

[0014] Moreover, the yield of a silicon integration process is not constant over time, since it is dependent on the actions performed to improve both the process characteristics and the circuit functional aspects. Typically, the yield is comparatively low at the start of the manufacturing process, to then improve as the production volume increases following to the process optimising actions.

[0015] For example, with a well developed integration technology widely employed for mass production, the yield

may attain its highest possible levels.

[0016] Of course, it is important to keep the manufacturing yield in memory devices high, possibly also from the very start of the manufacturing process.

[0017] In addition, every increase of the corrective capability of a redundancy architecture associated with a matrix of memory cells provokes an increase of the required area for its control circuitry, as well as an increase of the weight of the whole device complexity.

[0018] This added complexity becomes a serious problem with the row redundancy techniques, which heavily penalise, moreover, the access time to a memory word.

[0019] Thus, prior approaches provide optimal designed architectures for a given degree of the corrective capability, which degree is, therefore, fixed and unvaried for all the devices being manufactured.

[0020] In practice, implementing specific solutions with a high corrective capability involves an unacceptable longer time for accessing memory words, besides an increase in silicon area occupation, because of the complex control arrangements required.

[0021] One prior architecture aimed to reduced the access time of high corrective capability solutions making use of redundant rows is schematically shown in Figure 1.

[0022] Particularly, the architecture 1 comprises a matrix 2, called matrix sector, of memory cells which are organised into regular rows and columns, a row decoder block 3, and a column decoder block 4, as well as a read block 5.

[0023] The read block 5 comprises basically read circuits (sense amplifiers) and output buffers.

[0024] The architecture 1 further comprises at least one matrix 6 of redundant cells, called redundancy sector, operative to correct bit-fails spread with equal probability over all the sectors of matrix 2.

[0025] The architecture 1 finally comprises a memory 7 of the UPROM type for row redundancy.

[0026] It should be considered that in a flash memory device, such as that forming the subject matter of the above patent application, there are usually many sectors of memory cells having predetermined capacity. In fact the storage capacity of the sectors can be constant for all sectors or vary between sectors.

[0027] This organisation in sectors allows each cell matrix to be accessed separately for read, program and erase operations. In particular, whereas a program operation is selective of byte/memory words for any memory sector, an erase operation is shared by all the cells of each selected sector.

[0028] Selective access to the sectors is, therefore, achieved by providing a row or a column type of organisation of the sectors themselves and a physical separation of the source lines of each sector.

[0029] In particular, with a by-row organisation, the columns are distributed among all the sectors, and the selection takes place by row address, whereas in a dual manner, with a by-column organisation, the rows are distributed among all the sectors and the selection takes place by column address.

[0030] Furthermore, the by-row or by-column organisation of the matrix sectors can be performed by using single or double silicon level technologies. With a by-row organisation, rows shared by the sectors are realised in low-resistivity polysilicon, whereas the columns are realised in metal, while with a by-column organisation, a second metal level can be used to lower the overall resistance of the polysilicon rows, superposing the metal layer in contact with the polysilicon rows.

[0031] In processes with at least two metal levels, the matrix sectors can be organised in a combined by-row and by-column way. In this case, the row (column) decoding can use a hierarchic organisation based on "global" rows (columns), or rows shared by all the sectors to which the local rows (columns) of the individual sectors are connected. The local rows (columns) are particularly enabled only for a selected sector.

[0032] A hierarchic organisation of this type (by the rows or the columns) has a major advantage in that the effects of electric noise on the shared lines between adjoining cells under the different operating conditions are reduced, since the local bit lines or local word lines are shared by the cells of the single sectors.

[0033] By using a technological process with at least three metal levels, hierarchic decoding at the same time of the row and of the column is made feasible. In fact, in such a process, the global rows are realised with a first metal level, while the local rows are realised by low-resistivity polysilicon; the global and local columns are instead realised with a second and a third metal level, respectively.

[0034] In a conventional architecture 1 as just described, faulty cells are spotted at the device EWS (Electrical Wafer Sorting) stage. In the presence of faulty cells, an associative memory 6, also shown schematically in Figure 1, is controlled by on-chip control circuitry to allow a full matrix row "replacement" with a redundant row, in such a way that the access to the latter will be fully transparent to the ultimate user.

[0035] This replacement operation comprises storing the address of the faulty row permanently into non-volatile memory cells of the UPROM (Unerasable Programmable Read-Only Memory) type of the associative memory 6.

[0036] It should be specified that the term UPROM belongs to an EPROM technology wherein the UPROM cells are realised in a different manner from the memory cells, to avoid to erase them during exposure to UV radiation. On the other hand, with a flash technology, the erase operation is of the electrical type, and therefore the UPROM cells realised with such technology are actually identical to the memory cells. Nevertheless, it has become commonplace to use the

term UPROM to indicate memory cells employed for storing redundant addresses, as well as in the instance of flash technology.

[0037] With the conventional architecture 1, the redundant lines can be predecoded by the same row decoding signals of the memory matrix sectors 2, thus achieving a compromise between the corrective capability of the redundancy employed and silicon area occupation.

[0038] The solution illustrated by Figure 1 refers to flash technology implemented with a single or double metallization level technology, with hierarchic column decoding (hierarchic row decoding being non-limitative in application), with redundant cells provided in an associative memory, or rather in a redundant row sector 6, and with a shared source line.

[0039] In particular, the common source terminal of the redundant sector is associated with that of the sector which contains faulty cells. This condition is vital to the application because the architecture of a flash memory provides for the redundant cells to be erased simultaneously with those of their related sector.

[0040] The time for accessing a memory word in an architecture based on row redundancy is usually longer than that provided by architectures that do not employ such technique, due to the additional time required for redundancy handling (including comparing the row addresses, selecting a redundant row, etc.). This time is of about 10ns for conventional memory devices and is inclusive of delay in the propagation of signals over interconnecting lines because of the less-than-ideal effects relating to their physical implementation.

[0041] Access time, moreover, is longer in a row redundancy architecture than in a column redundancy architecture, due to the different organisation of the memory matrix in either cases.

[0042] In particular, in multimegabit flash memory devices exhibiting high parallelism during a burst read mode, the memory sectors are designed to include a significantly larger number of columns than of rows. Consequently, the row pre-charge time will be longer than the column time, mainly because of the increased RC load associated therewith.

[0043] For a given line load, pre-charge time is proportional to the final voltage sought; in case of reading with a higher gate voltage than the supply voltage Vdd (as in the case of multi-level memories or conventional two-level memories using a so-called gate-boosted reading technique), the penalty is heavier on access time because row pre-charging takes longer.

[0044] In order to minimise the effect on access time, the prior solution under consideration provides with a simultaneously pre-charging of both the selected and the redundant row, even where the former does not require to be replaced, at every change of address forced from outside. The evaluation of the redundant event for the selected row is carried out during the row pre-charging time, while the local columns are deselected. In this way, uniformity of access time can be achieved for both devices provided with redundancy and devices which are not provided with redundancy.

[0045] In summary, this prior architecture does enhances the corrective capability of the whole device for only a predetermined number of redundant rows, by virtue of the matrix of memory cells having hierarchic decoding features, in particular of the redundant rows being organised within a dedicated sector with local column decoding.

[0046] This particular hierarchic decoding architecture provides, therefore, for optimum handling of row redundancy, maximising corrective capability without penalty on memory word accessing time. In fact, with this architecture, some functional operations can be arranged to overlap in time, thus reducing the access time to the memory words. The architecture is, therefore, of special advantage with memory devices wherein the time required for pre-charging a selected row is longer than the time for sensing the redundancy event of such a row.

[0047] However, the prior solutions are advantageous at the initial stage of the manufacturing process, being justified by the need to obtain a high yield, and become gradually less useful, as the yield improves with the manufacturing process becoming more favourable over time.

[0048] The underlying technical problem of this invention is to provide a memory architecture having row redundancy control, with such structural and functional features as to afford chip-by-chip re-configurability of the architecture corrective capability, thereby overcoming the drawbacks and limitations of prior art memory architectures.

[0049] Thus, the capability to recover faulty cells can be adjusted to fill actual demands during the fabrication of the architecture, achieving the best compromise between the corrective capability of the architecture and its effect on access time to the memory words of a cell matrix with which the architecture is associated.

Summary of the Invention

[0050] The principle of this invention is one of configuring each device product at the EWS stage of its fabrication.

[0051] Based on this principle, the technical problem is solved by a configurable row redundancy memory device as previously indicated and defined in the characterising part of Claim 1.

[0052] The features and advantages of the device according to the invention can be more clearly understood by reading the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

[0053] In the drawings:

- Figure 1 schematically shows a memory device with redundancy, according to the prior art;
- Figure 2 schematically shows a memory matrix with row redundancy, according to the invention;
- Figures 3A and 3B show the memory matrix of Figure 2 in greater detail;
- Figure 4 schematically shows a detail of the memory matrix of figure 2;
- Figure 5 schematically shows a device incorporating a memory matrix with row redundancy according to the invention.

Detailed Description

[0054] The following description deals with non-volatile flash memory devices for illustration purposes, it being understood that the expounded considerations equally apply to memory devices of the EPROM or the EEPROM type.

[0055] Referring to the drawing views, and particularly to Figure 6, a memory architecture with hierarchic row and column redundancy, according to the invention, is schematically shown generally at 10.

[0056] It should be noted that the described architecture is but a non-limitative example of the organisation of a memory having hierarchic row and column redundancy. In particular, the architecture 10 comprises a predetermined number Ns of matrix sectors and a predetermined number Nr of redundant rows.

[0057] In particular, the architecture 10 is organised into both rows and columns, whereby any sector of such architecture shares rows and columns with each sector lying adjacent to it.

[0058] The memory architecture 10 comprises nxm memory sectors, it being nxm=Ns, which are organised as vertical groups of sectors, designated V1, V2...Vn, and horizontal sector groups, designated H1, H2...Hm.

[0059] Each vertical sector group V1, V2...Vn is associated with at least one row redundancy sector.

[0060] For the sake of simplicity, it will be considered hereinafter that a single redundancy sector is provided for each vertical group, being designated R1, R2...Rn. In practice, a larger number of redundancy sectors can be associated with a single vertical sector group, thereby expanding the corrective capability of the memory architecture 10.

[0061] The memory architecture 10 comprises a matrix 11 of memory cells, particularly consisting of the vertical V1, V2...Vn and horizontal H1, H2...Hm groups of memory sectors, the redundancy sectors R1, R2...Rn, global row 12 and column 13 decoders, and an associative matrix 14.

[0062] In particular, a row address ADr is supplied to the row decoder 12 and the associative memory matrix 14, the latter being connected to the row and column decoders, 12 and 14.

[0063] The architecture 10 of this invention employs, for example, a local column decoding facility for both the matrix and the redundancy sectors, such type of decoding facility being neither essential to, nor limitative of, the proposed solution, but merely a preferred embodiment. For simplicity, the local decoding blocks are omitted from the drawing because of no characterising value to the invention purposes.

[0064] In the organisation shown in Figure 2, each sector row is replaced only by a redundant row having the same pre-decoding signals corresponding to it. In addition, to maximise corrective capability for a predetermined number of redundant rows, the number of the sector row decoding signals is set equal to that of the redundant row select signals.

[0065] For such purpose, the source lines of the redundant cells are connected with each other, and electrically connected to a voltage generator through a selector circuit, not shown.

[0066] When using CMOS technologies, the rows of the flash cell matrices are formed in low-resistivity polysilicon. In technological processes providing for two or three metal levels, the polysilicon lines can be parallel connected to metal lines in order to reduce the overall parasitic resistance of the rows and, hence, the propagation delays, according to a technique known as wordline metal strapping.

[0067] In any case, the conductive layers providing the matrix rows have to be formed within the wordline pitch, that is, placed at submicron distances from one another.

[0068] This feature of the architecture makes two rows being in physical contact with each other a statistically likely event apt to result in the creation of shorts at one or more spots.

[0069] With current integration technologies providing a high degree of control of the lithographic patterning, the spread of faults from the row conductive layers becomes restricted to isolated punctual regions of the matrix. Furthermore, faultiness is higher in the polysilicon lines than the metal-polysilicon lines.

[0070] In general, the use of such techniques as the aforementioned metal strapping, in combination with currently

available technologies, can bring faultiness to such a low level that redundancy techniques becomes unnecessary.

[0071] Actually, increased levels of faultiness appear at the start of the manufacturing process, and justify the application of a row or column redundancy technique. It is often necessary, in actual practice, to recover a row or a small group of adjoining rows due to local faultiness from the technological process.

[0072] As regards the application of the memory architecture 10 of this invention, two separate cases should be considered:

1) two faulty rows scattered within the same sector occur in Ns sectors;

2) more than two faulty rows scattered in different sectors occur in Ns sectors.

[0073] It should be noted that a minimum target of the redundancy technique is the replacement of a fault in a row which is equally likely to be spread through all the rows of the matrix 11; a general target of maximum coverage is instead the correction of a larger number of row faults, located everywhere.

[0074] The memory architecture 10 of this invention practically affords increased corrective capability since, in the general case, a redundant sector Ri (i=1, 2,...,n) can be used to replace just the faulty rows belonging only to the corresponding vertical sector group Vi, as shown in Figures 3A and 3B.

[0075] In particular, this architecture 10 with row redundancy provides two main fault coverages, in a configurable style:

1.1) n/n;

2.1) 1/n.

[0076] In practice, for a memory architecture having Ns=64 memory sectors arranged in n=8 vertical groups and m=8 horizontal sector groups, the configurable corrective capability of an architecture according to the invention is:

1.1) 8/8 recoverable faults from a single sector of 64 sectors;

2.1) 1/8 independently recoverable faults from a single sector of 8 sectors.

[0077] Figure 3 schematically shows, by way of example, an organisation of the memory 10, with minimum coverage of 8/8 and maximum coverage of 1/8 for a predetermined number (8) of redundancy sectors.

[0078] Architectures can be likewise implemented with corrective capability in between 8/8 and 1/8. For example, it is possible to cover faults located in groups of 16 or 32 sectors (corrective capability of 1/4 and 1/2, respectively).

[0079] The choice of the solution to be applied is dependent on the compromise between the corrective capability and the silicon area required by the architecture 10, in particular dependent on the UPROM circuitry associated with the redundancy. In selecting the corrective capability, its effect on the access time to a memory word is also taken into account.

[0080] The information about the addresses of faulty rows is stored into non-volatile memory cells included in associative memory matrix 14 which receives at its input the row address ADr and has its output connected to the decoding blocks 12 and 13.

[0081] In particular, each row of the associative memory matrix 14 contains the addresses of the faulty rows of a single sector of a given vertical sector group. Thus, the number of columns varies according to the spare rows available for each sector, as schematically shown in Figure 4.

[0082] Figure 4 shows an associative memory matrix 14, organised, for example, into 8 rows and addressed by means of a dedicated row decoder 15. In particular, a cell address AD is split into a vertical group address ADv which is sent to the dedicated row decoder 15, and a row address ADr which is sent to logic control circuitry 16.

[0083] A row address ADrr of the associative memory matrix 14 is then compared with the current row address ADr by the logic control circuitry 16, which outputs a redundancy event signal RE. In particular, if the current row signal ADr happens to be the same as the redundant row signal ADrr, a positive redundancy event RE is signalled effective to control the replacement of faulty rows in a memory matrix 11 associated with the associative memory matrix 14.

[0084] Of course, with the architectural layout shown in Figure 4, only one row at a time of the associative memory matrix 14 can be selected, as is the case with conventional NORed memory architectures. Thus, at each change of row in the associative memory matrix 14, the corresponding memory cells in the memory matrix 11 are read and their addresses compared once again.

[0085] It should be noted that, in the instance of 8/8 coverage, bit-fail situations are present only in the same sector within the memory matrix 11.

[0086] Accordingly, the positions of faulty rows can be identified during the memory testing and stored into the associative memory matrix 14, using the corresponding portion of the memory address. In this case, a single row of the associative memory matrix 14 is sufficient to store the addresses of the faulty rows, since the latter can only belong to the same vertical sector group.

[0087] In particular, this information about the faulty rows can be read cumulatively at the device power-up, or where so provided, during the hardware resetting phase, when an impulse of a predetermined minimum duration is usually applied to a reset pin.

[0088] On the other hand, with a 1/8 coverage, bit-fail situations may be present in sectors belonging to different groups of vertical sectors. But in each vertical group, only one sector can be corrected at most. Such faulty row information is, therefore, read by means of an ATD signal normally provided in circuitry associated with a memory architecture.

[0089] In this case, the corrective capability of the memory architecture of this invention is multiplied by a factor equal to the number of vertical sector groups.

[0090] The situations in the above extreme cases can be summarised as follows:

Organisation	Coverage	Associative matrix reading
8/8	1 sector/64	Reset
1/8	1 sector/8	ATD

[0091] A non-volatile memory device with configurable row redundancy is schematically shown in Figure 5 and indicated with 20.

[0092] The memory device 20 comprises:

- a non-volatile memory 11 consisting of at least one matrix 11' of memory cells and at least one matrix 11" of redundant memory cells, both organised in the row and column form;
- row 12 and column 13 decoding circuits;
- read and modify circuits for reading and modifying the data stored in the memory cells (not shown because conventional); and
- at least one associative memory matrix 14, also organised in the row -
- and column form, wherein the addresses of faulty rows can be stored, and associated control circuits therefor.

[0093] Advantageously in the invention, the memory device 20 further comprises:

- at least one circuit for recognising and comparing selected row addresses ADr with faulty row addresses ADrr contained in the associative memory matrix 14, which circuit can produce de-selection of a faulty row and selection of a corresponding redundant cells row in the event of a valid recognition: and
- at least one configuration register 17, also comprising a matrix of non-volatile memory cells, and associated control circuits.

[0094] In particular, the associative memory matrix 14 receives the row address signal ADr, and is connected to the row decoder 12 and the configuration register 17.

[0095] Advantageously in the invention, this configuration register 17 is programmed, at the ESW stage, with the performance of the associative memory redundancy matrix 14.

[0096] The memory device 20 is then completed with a sense amplifier 18 arranged to generate a data output signal OUT.

[0097] Information is read from the associative memory matrix 14, during reading or programming operations of a memory word from/into a matrix, in two different ways:

- only once during recovery at the reset or power-up stages of the device (8/8 coverage, for example);
- at each change of access address by means of an ADT signal (1/8, 1/4, 1/2 coverages, for example).

[0098] During erase operations of a cell matrix, the information read in the associative memory matrix 14 is made only on the matrix address information.

[0099] It should be noted that the memory device 20 according to the invention has column decoding of the hierarchic type, i.e. has a number of main columns which are shared by the memory cell matrix 11' and the redundant cell matrix 11", and has a number of independent local columns for each matrix.

[0100] In addition, the cell matrices 11' and 11" share global rows and columns with their adjoining matrices, so that the device would include at least one vertical group of non-volatile memory cell matrices and at least one redundant cell matrix (as previously described in relation to Figure 2).

[0101] In particular, the redundant rows are provided in the dedicated associative memory matrix 14, having local column decoding facilities, while row decoding may be of the conventional or of the hierarchic type. Furthermore, there is at least one row redundancy matrix provided for each vertical group of matrices.

[0102] As previously described, a given cell matrix is selected by an address which has a portion for selecting a vertical group of matrices, to which such matrix belongs, and a portion for selecting that matrix among a specific vertical group of matrices.

[0103] Advantageously in the invention, each row of the associative memory matrix 14 is, moreover, selected univocally by an address of at least one vertical group of cell matrices, according to the corrective capability of the matrix.

[0104] To summarise, the proposed solution has the following advantages, whereby:

- possibility to configure chip-by-chip the corrective capability of the faulty rows, which can be replaced with identical redundant rows;
- the corrective capability can be set at the ESW stage by programming specially dedicated configuration bits into the configuration register 17;
- the effect of redundancy on the access time to the memory words can be minimised, this time being only dependent on the evaluation of the redundancy event as a function of the corrective capability of choice (becoming even zero with full coverage).

[0105] Furthermore, the fact deserves to be underlined that the memory device 20 of this invention has two different modes of operation:

- activation of the address comparison during the device resetting [power-on reset or hardware reset] operations, where all the faulty rows are contained in one cell matrix at most of a single vertical group of matrices;
- activation of the address comparison during each read operation, where all the rows available for redundancy belong to at least two distinct cell matrices in different vertical groups of matrices.

[0106] In addition, by providing the configuration register 17, these modes of operating the associative memory matrix 14 become functions of the informational contents of this register, which contents can be stored independently chip-by-chip.

[0107] It is further possible to operate the memory device 20 in the following modes:

- activating, at each read or program operation of a memory cell, the comparison of the row address where the memory cell locates and the contents of a given row of the associative memory matrix 14;
- at each erase operation of a memory matrix, activating the comparison between the address of the memory matrix and the contents of a given row of the associative memory matrix 14.

Claims

1. A non-volatile memory device (20) with configurable row redundancy, comprising:
   - a non-volatile memory (11), itself comprising at least one matrix (11') of memory cells and at least one matrix (11") of redundant memory cells, both organised into rows and columns;
   - row and column decoding circuits (12,13);

- read and modify circuits for reading and modifying data stored in the memory cells; and

- at least one associative memory matrix (14), also organised into rows and columns, able to stor the addresses of the faulty rows, and control circuits for controlling the associative memory matrix;

characterised in that it further comprises:

- at least one circuit for recognising and comparing selected row addresses (ADr) with faulty row addresses (ADrr) contained in the associative memory matrix (14), such as to produce de-selection of the faulty row and selection of the corresponding redundant cell row in the event of a valid recognition; and

- at least one configuration register (17), also comprising a matrix of non-volatile memory cells, and associated control circuits.

2. A non-volatile memory device (20) with configurable row redundancy according to Claim 1, characterised in that said configuration register (17) is programmed, at an initial testing stage of the device, with the performance of the redundancy associative memory matrix (14).

3. A non-volatile memory device (20) with configurable row redundancy according to Claim 1, characterised by having main cell columns shared by the memory cell matrix (11') and the redundant cell matrix (11"), and having independent local columns for each matrix, so that a hierarchic type of column decoding is implemented.

4. A non-volatile memory device (20) with configurable row redundancy according to Claim 3, characterised in that said cell matrices (11',11") share global rows and columns with adjoining matrices, so that said memory (11) comprises at least one vertical group of cell matrices and at least one redundant cell matrix.

5. A non-volatile memory device (20) with configurable row redundancy according to Claim 4, characterised in that a given cell matrix is selected by an address comprising a portion which selects a vertical group of matrices containing said given matrix and a portion which selects said given matrix in a determined vertical group of matrices.

6. A non-volatile memory device (20) with configurable row redundancy according to Claim 1, characterised in that each row of the associative memory matrix (14) is selected univocally by an address of at least one vertical group of cell matrices according to the corrective capability of the matrix.

7. A non-volatile memory device (20) with configurable row redundancy according to Claim 1, characterised in that the information is read in the associative memory matrix (14), during the operations of reading or programming a memory word in a matrix, in two different ways:

- only once, upon recovery at the device (20) setting stage;

- at each change of access address by means of an appropriate drive signal (ATD).

8. A non-volatile memory device (20) with configurable row redundancy according to Claim 1, characterised in that it includes circuits for controlling the associative memory matrix (14) according to two different modes of operation:

- activating the address comparison during the device (20) resetting operations, where all the faulty rows belong at most to one cell matrix of a single vertical group of matrices;

- activating the address comparison during each read operation, where all the rows available for redundancy belong to at least two distinct cell matrices of different vertical groups of matrices.

9. A non-volatile memory device (20) with configurable row redundancy according to Claim 8, characterised in that said operating modes of the associative memory matrix (14) are functions of the contents of said configuration register (17).

10. A non-volatile memory device (20) with configurable row redundancy according to Claim 9, characterised in that the contents of said configuration register (17) can be stored independently on a chip-by-chip basis.

11. A non-volatile memory device (20) with configurable row redundancy according to Claim 9, characterised in that it includes circuits for controlling the associative memory matrix (14) for two distinct modes of operation:

- activating, at each read or program operation of a memory cell, the comparison between the row address to which the memory cell belongs and the contents of a given row of the associative memory matrix (14);

- activating, at each erase operation of a memory matrix, the comparison between the address of the memory matrix and the contents of a given row of the associative memory matrix (14).

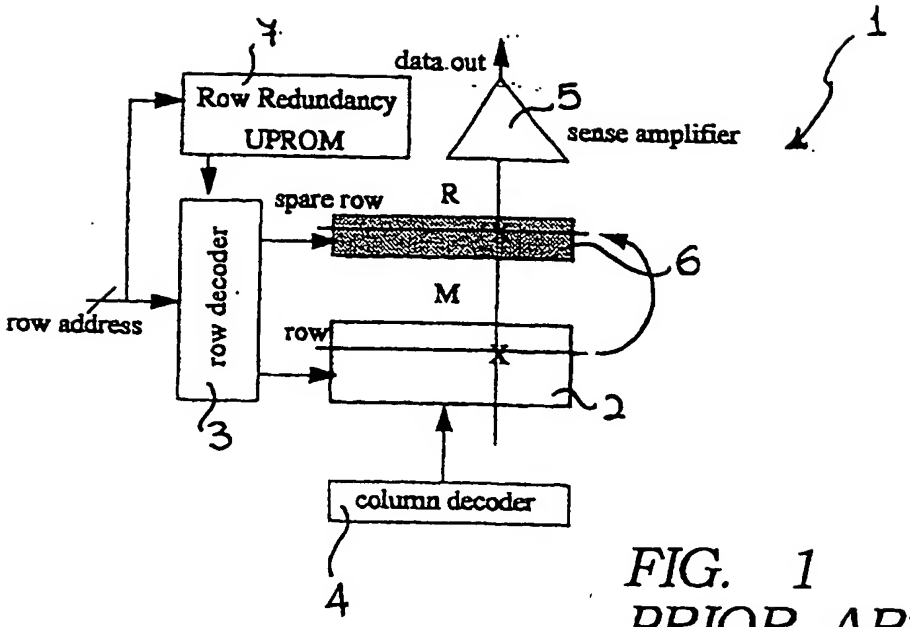

FIG. 1
PRIOR ART

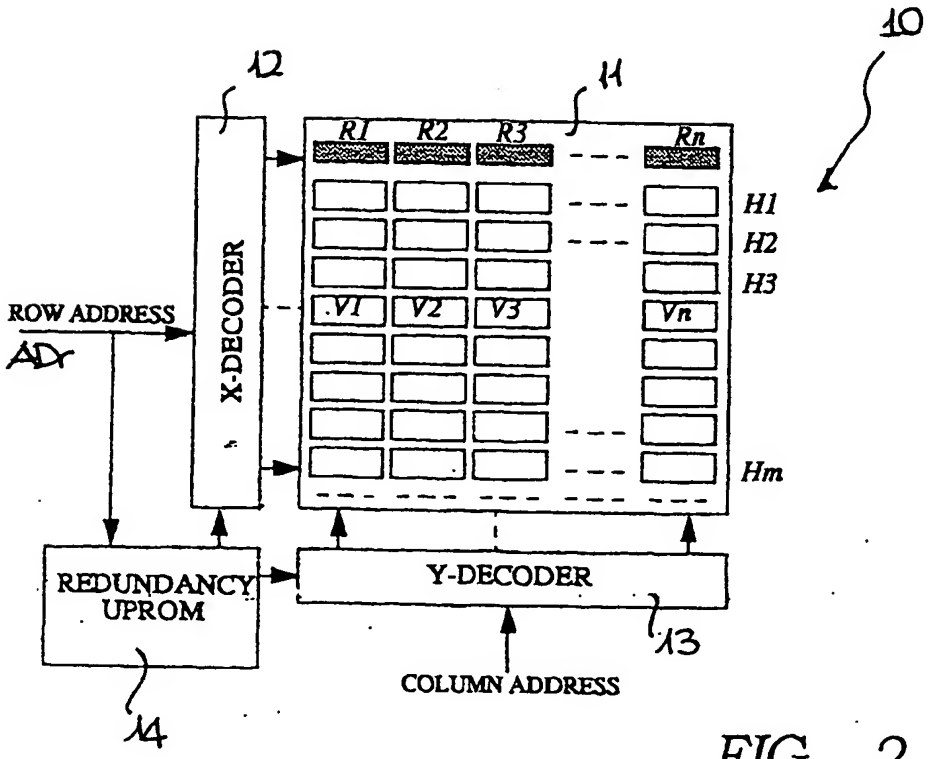

FIG. 2

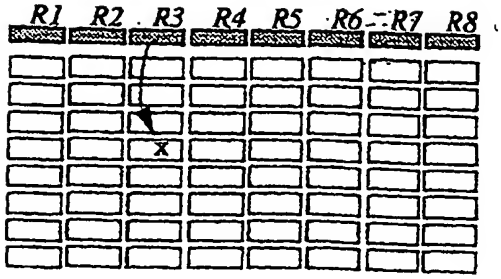

FIG. 3A

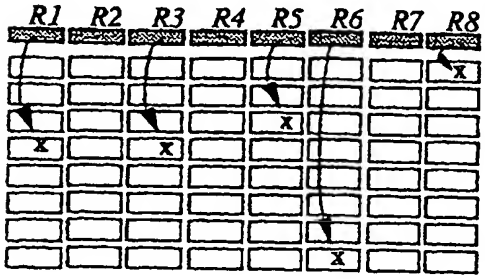

FIG. 3B

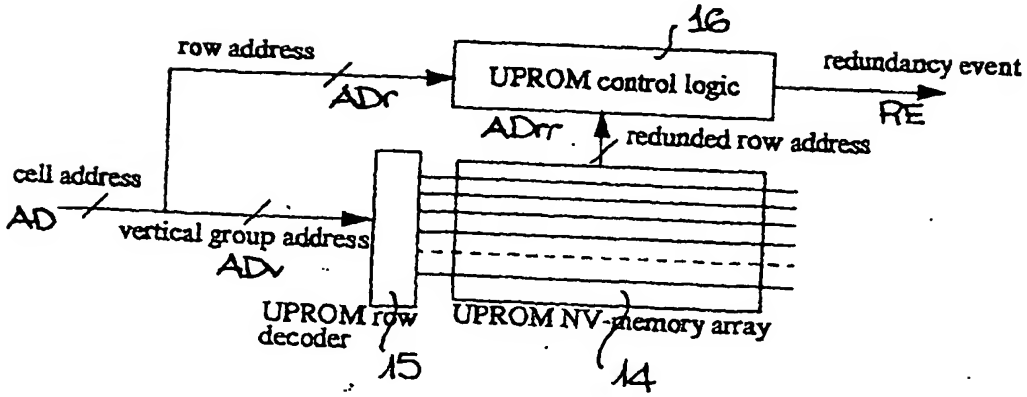

FIG. 4

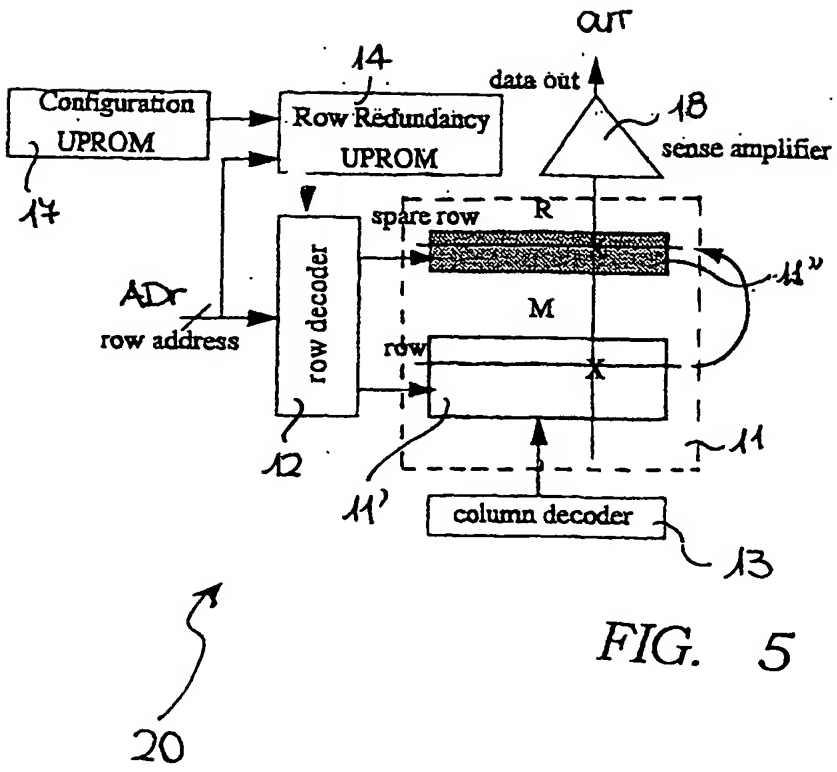
OUT
14
data out
18
sense amplifier
Configuration
UPROM
Row Redundancy
UPROM
17
spare row
R
row decoder
ADr
row address
M
row
X
11"
12
11'
11
column decoder
13
20

FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0103

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A	US 6 018 482 A (FUJITA MAMORU) 25 January 2000 (2000-01-25) * column 5, line 36 - column 6, line 3 * * column 8, line 26 - line 46 *	1-3,6-8	
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G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 July 2000	Fernandez Balseiro,J

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